

Appl. No. 09/676,311  
Amdt. dated March 19, 2004  
Reply to Office Action of November 19, 2003

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended):

A method of handling memory errors comprising:

receiving and retaining control of a machine from an executing program after an error in a memory value is detected while executing a memory load request issued by the executing program to retrieve a the memory value from the memory;

receiving a speculative load indication that is true if the memory load request was issued speculatively;

reading a fault deferral indication that is true if faults caused by errors in memory values can be deferred, the fault deferral indication being set before the error in the memory value is detected;

if the fault deferral indication is true and the speculative load indication is true, providing an error indication that the returned memory value from the memory is invalid; and,

returning control of the machine to the executing program.

2. (currently amended):

The method of claim 1, wherein the error indication is a flag bit associated with the returned memory value.

3. (currently amended):

The method of claim 1, wherein the error indication is setting the returned memory value to an invalid value.

4.-5. (canceled)

6. (previously presented):

A machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform operations comprising:

receiving and retaining control of a machine from an executing program after an error in a memory is detected while executing a memory load request issued by the executing program to retrieve a value from the memory;

receiving a speculative load indication that is true if the memory load request was issued speculatively;

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reading a fault deferral indication that is true if faults can be deferred, the fault deferral indication being set before the error in the memory is detected;  
if the fault deferral indication is true and the speculative load indication is true, providing an error indication that the returned value from the memory is invalid; and,  
returning control of the machine to the executing program.

7. (original):

The machine-readable medium of claim 6, wherein the error indication is a flag bit associated with the returned value.

8. (original):

The machine-readable medium of claim 6, wherein the error indication is setting the returned value to an invalid value.

9.-10. (canceled)

11. (previously presented):

A machine comprising:

an interface to receive a value from a memory coupled to the machine;  
a speculative load indicator that is true if the memory load request was issued speculatively; and  
a fault deferral indicator that is true if faults can be deferred, the fault deferral indicator being set before the error in the memory is detected;  
a machine-readable medium that provides instructions, which when executed by the machine, cause the machine to perform operations including  
receiving and retaining control of the machine from an executing program after an error in the memory is detected while executing a memory load request issued by the executing program to retrieve a value from the memory;  
if the fault deferral indicator is true and the speculative load indicator is true,  
providing an error indication that the returned value is invalid; and,  
returning control of the machine to the executing program.

12. (original):

The machine of claim 11, wherein the machine further comprises a register to receive the value, and a flag bit associated with the register, wherein the error indication is a defined value of the flag bit.

13. (original):

The machine of claim 11, wherein the machine further comprises a register to receive the value, and the error indication is an invalid value in the register.

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14.-15. (canceled)

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16. (previously presented):

A system comprising:

a machine;

a memory coupled to the machine; and

a machine-readable medium that provides instructions, which when executed by the machine, cause the machine to perform operations including

receiving and retaining control of the machine from an executing program after an error in the memory is detected while executing a memory load request issued by the executing program to retrieve a value from the memory,

reading a fault deferral indication that is true if faults can be deferred, the fault deferral indication being set before the error in the memory is detected;

receiving a speculative load indication that is true if the memory load request was issued speculatively,

if the fault deferral indication is true and the speculative load indication is true, providing an error indication that the returned value from the memory is invalid; and,

returning control of the machine to the executing program.

17. (original):

The system of claim 16, wherein the machine further comprises a register to receive the value, and a flag bit associated with the register, wherein the error indication is a defined value of the flag bit.

18. (original):

The system of claim 16, wherein the machine further comprises a register to receive the value, and the error indication is an invalid value in the register.

19.-20. (canceled)